In the Claims:

Please amend claims 2, 3, 5, 7, 15-23 and 27-29. Please cancel claims 1, 4, 6, 8-13, 24-26 and 30. Please add new claims 32 and 33.

The claims are as follows:

1. (Canceled)

2. (Currently Amended) The computer system of claim [[1]] 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said switch and connected to ~~one of said~~ a respective I/O driver models.

3. (Currently Amended) The system of claim [[1]] 31, wherein said simulated external memory mapped test device further includes [[an]] a simulated address register.

4. (Canceled)

5. (Currently Amended) The system of claim 2, wherein each said simulated external memory mapped test device module further includes [[an]] a simulated address register.

6. (Canceled)

7. (Currently Amended) The system of claim [[1]] 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to ~~one of said~~ a respective I/O driver model[[s]] of said one or more I/O driver models and further including the method steps of :

providing an additional simulated external memory mapped test device module;

~~directly connected to~~ connecting one or more additional I/O driver models to said additional simulated external memory mapped test device by additional simulated I/O buses ; ~~each~~ ; and

connecting each additional I/O driver model ~~directly connected~~ to ~~an~~ a respective additional simulated I/O core by said simulated system bus, each additional simulated I/O core ~~part of~~ comprising said model of integrated circuit design.

8-13 (Canceled)

14. (Previously Presented) A method for verifying an integrated circuit design comprising:

providing an I/O controller connected to one or more I/O cores, said I/O cores part of said integrated circuit design;

providing an external memory mapped test device having a switch for selectively connecting one or more of said I/O cores to corresponding I/O driver models;

providing a bus for transferring signals between said I/O controller and said switch;

providing a test operating system for controlling said switch;

simulating said integrated circuit design by running a test case on said test operating system;

distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models: and

providing an additional external memory mapped test device module directly connected to one or more additional I/O driver models, each additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design.

15. (Currently Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for verifying an integrated circuit design, said method steps comprising:

providing a simulated external memory mapped test device software module having a simulated switch programmably connectable to one or more simulated I/O drivers ~~models~~ and to a simulated I/O controller, said simulated I/O drivers ~~models~~ connected to corresponding simulated I/O cores by corresponding ~~virtual~~ simulated I/O buses;

providing a simulated virtual memory bus connecting said simulated I/O controller and said simulated switch;

programming connections of said simulated external memory mapped test device and connections of a simulated general purpose I/O core to said simulated I/O models;

wherein said simulated I/O cores, said simulated general purpose I/O core and said simulated I/O controller ~~are software descriptions~~ comprise a computer model of said integrated circuit design; and

simulating said computer model of said integrated circuit design by running a test case with said programmed connections.

16. (Currently Amended) The program storage device of claim 15, said method steps further including:

distributing said simulated external memory mapped test device and said simulated switch among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory modules containing a portion of said simulated switch and connected to one of said simulated I/O driver models.

17. (Currently Amended) The program storage device of claim 15, said method steps further including:

providing said simulated external memory mapped test device with [[an]] a simulated address register; and setting said simulated switch and controlling said simulated I/O driver using address information programmed into said simulated address register.

18. (Currently Amended) The program storage device of claim 15, said method steps further including:

providing [[an]] a simulated embedded processor in said simulated model of said integrated circuit design, said embedded simulated embedded processor running said test operating system ~~controlling said software~~.

19. (Currently Amended) The program storage device of claim 16, said method steps further including:

providing each simulated external memory mapped test device with [[an]] a simulated address register; and

setting each portion of said simulated switch and controlling each simulated I/O driver using address information programmed into said simulated address register.

20. (Currently Amended) The program storage device of claim 16, said method steps further including:

providing said simulated model of said integrated circuit design with [[an]] a simulated embedded processor running said test case on said simulated embedded processor.

21. (Currently Amended) The computer system of claim [[1]] 31, wherein said one or more simulated I/O cores ~~are independently selected from the group consisting of~~ includes a simulated 1394 I/O core[[s]], a simulated universal asynchronous receiver transmitter core[[s]], a simulated serial cores, ~~and~~ a simulated general purpose I/O core[[s]] or combinations thereof.

22. (Currently Amended) The computer system of claim [[1]] 31, wherein said integrated circuit design further includes ~~an embedded processor core,~~ a memory controller core and a direct memory access core.

23. (Currently Amended) The computer system of claim 22, said computer simulation model of said integrated circuit design further including a simulated direct memory access core model of said [[a]] direct memory access core.

24-26 (Canceled)

27. (Currently Amended) The program storage device of claim 15, wherein said one or more simulated I/O cores ~~are independently selected from the group consisting of~~ includes a simulated 1394 I/O core[[s]], a simulated universal asynchronous receiver transmitter core[[s]] ~~and~~ a simulated serial core[[s]] or combinations thereof.

28. (Currently Amended) The program storage device claim 15, wherein said computer model of said integrated circuit design includes [[an]] a simulated embedded processor core, a simulated memory controller core ~~and~~ , a simulated direct memory access core or combinations thereof.

29. (Currently Amended) The program storage device of claim 27, wherein said computer model of said integrated circuit design includes a simulated direct memory access core model of ~~said~~ a direct memory access core of said integrated circuit design.

30. (Canceled)

31. (New) A computer system comprising a processor, an address/data bus coupled to said processor, and a computer-readable memory unit coupled to communicate with said processor,

said memory unit containing instructions that when executed by the processor implement a method for verifying an integrated circuit design, said method comprising the computer implemented steps of:

providing a simulated external memory mapped test device having a simulated switch programmably connectable to one or more I/O driver models and to a simulated I/O controller, said I/O driver models connected to corresponding simulated I/O cores by corresponding simulated I/O buses, said simulated I/O cores and said simulated I/O controller connected to a simulated processor by a simulated system bus, said simulated I/O cores, said simulated I/O controller, said simulated bus system and said simulated processor comprising a computer simulation model of said integrated circuit design; and

loading a test case comprising a list of computer-executable instructions for verifying said integrated circuit design into said simulated external memory mapped test device and executing said computer-executable instructions on said simulated processor in order to generate data representing a response of said computer simulation model of said integrated circuit design to said test case.

32 (New) The system of claim 31, wherein said simulated external memory mapped test device and said I/O driver models do not comprise said model of said integrated circuit design.

33. (New) The system of claim 31, wherein said simulated external memory mapped test device and said one or more I/O driver models comprise a computer simulation model of a test system.